JAPANESE [JP,08-008247,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS OPERATION EXAMPLE DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The semiconductor device characterized by having a wiring of the multilayer structure in which the 2nd layer which consists of an insulator was formed on the 1st layer which consists of the metallic compounds or the alloy which makes a metal or the aforementioned metal a principal component.

[Claim 2] It is the semiconductor device according to claim 1 characterized by for the 1st aforementioned layer consisting of the metallic compounds or the alloy which makes a principal component any one metal or these metals at least among molybdenum (Mo), a tungsten (W), titanium (Ti), a tantalum (Ta), and chromium (Cr), and the 2nd aforementioned layer consisting of oxidization silicon or a silicon nitride.

[Claim 3] The 1st aforementioned layer is a semiconductor device according to claim 1 or 2 characterized by presenting from the bottom the multilayer structure which becomes order from molybdenum, gold (Au), and molybdenum.

[Claim 4] The 1st aforementioned layer is a semiconductor device according to claim 1 or 2 characterized by presenting from the bottom the multilayer structure which becomes order from a titanium tungsten (Ti W), gold (Au), and a titanium tungsten.

[Claim 5] The semiconductor device according to claim 1, 2, 3, or 4 characterized by the 2nd aforementioned layer thickness being 100nm or less.

[Claim 6] The 1st process which forms the 1st layer which consists of the metallic compounds or the alloy which makes a metal or the aforementioned metal a principal component on the insulator layer of a substratum, The 2nd process which forms the 2nd layer which consists of an insulator on the 1st aforementioned layer, The manufacture technique of the semiconductor device characterized by consisting of the 3rd process which forms the photoresist pattern for masks on the 2nd aforementioned layer, and the 4th process which uses the aforementioned photoresist pattern as a mask and processes the above 1st and the 2nd layer into a predetermined pattern.

[Claim 7] The manufacture technique of the semiconductor device according to claim 6 characterized by performing ion milling which uses the aforementioned photoresist pattern as a mask at the 4th aforementioned process.

[Claim 8] It is the manufacture technique of the semiconductor device according to claim 6 or 7 characterized by for the 1st aforementioned layer consisting of the metallic compounds which make a principal component any one metal or these metals among molybdenum (Mo), a tungsten (W), titanium (Ti), a tantalum (Ta), and chromium (Cr), and the 2nd aforementioned layer consisting of oxidization silicon or a silicon nitride.

[Claim 9] The manufacture technique of the semiconductor device according to claim 6, 7, or 8 characterized by the 2nd aforementioned layer thickness being 100nm or less.

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is applied to the semiconductor device which has the wiring pattern of multilayer structure, and its manufacturing technology about a semiconductor device and its manufacturing technology, and relates to effective technique.
[0002]
[Description of the Prior Art] It is the purpose of realizing the ohmic contact of the device and wiring which were formed in the front face of a compound semiconductor substrate in compound semiconductor elements, such as the former, for example, a gallium, and an arsenic (Ga As), and is Au as a wiring material. It is Au although using is known. The adhesion to insulator layers, such as oxidization silicon, is inferior. for this reason — for example, it is indicated by reference, such as issue, the Institute of Electronics and Communication Engineers study group data ED 81-122, and p46, in 1981 — as — Ga As a wiring of a semiconductor device — Ti-Au **** — the becoming multilayer structure is adopted Ti-Au A wiring is Ti in order to raise the adhesion with a lower layer insulator layer. It is used. Moreover, it is Ti-Au-Ti in order to raise the adhesion with the upper insulator layer similarly. A wiring and Mo-Au-Mo The structure of a wiring may be adopted.
[0003]
[Problem(s) to be Solved by the Invention] However, Mo of the upper layer exposed to a front face in the above conventional multilayer structure and Ti There was a problem that oxidized, it was simultaneously polluted with the elimination process of the photoresist by ashing (ashing processing by oxidization), washing, etc. in the middle of a manufacturing process, and a grade disappeared. For example, Mo Since the oxide is water-soluble, it will disappear easily at the washing process after ashing.
[0004] The purpose of this invention is to offer the semiconductor device which can prevent certainly sublation with a wiring of multilayer structure, and a upside insulator layer.
[0005] Other purposes of this invention are to offer the manufacturing technology of the semiconductor device which can prevent certainly sublation with a wiring of multilayer structure, and a upside insulator layer.
[0006] The purpose of further others of this invention is to offer the manufacturing technology of the semiconductor device which can perform sufficient photoresist elimination processing, without being anxious about trauma of a wiring etc.
[0007] The purpose of the above and others of this invention and the new characteristic feature will become clear from description and the accompanying drawying of this specification.
[0008]
[Means for Solving the Problem] It is as follows if the schema of a typical thing is briefly explained among invention indicated in this application.
[0009] the semiconductor device and its manufacturing technology of this invention — Mo, W, Ti, Ta, and Cr the 1st layer top which consists of the metallic compounds or the alloy which makes a principal component any one metal or these metals inside — for example, the 2nd layer which consists of a thin insulator layer is formed, and it considers as the wiring pattern

of multilayer structure Moreover, the ion milling which uses a photoresist as a mask can be used for a manipulation of this wiring pattern.
[0010]
[Function] Mo which is wiring, W, Ti, Ta, and Cr Since the 2nd layer which consists of an insulator layer formed on the 1st layer which consists of a metal of a grade functions as a protective coat of the 1st layer, it is prevented certainly that set at ashing and the washing process by the oxygen plasma in an elimination process of a photoresist, and the surface section of the 2nd layer oxidizes, pollutes and disappears. For this reason, for example, it is arranged at the top of the 1st layer which constitutes a wiring, disappearance of the metal thin film formed in order to raise the adhesion with the protection insulator layer formed in the concerned wiring bottom is prevented, and failure, such as sublation of a protection insulator layer and blistering, does not occur, but the yield of a semiconductor device improves certainly.
[0011]
[Example] Hereafter, the example of this invention is explained in detail based on a drawing.
[0012] The drawing 1 and the drawing 2 are abbreviation cross sections showing a part of semiconductor device which is one example of this invention, and its manufacture technique in the order of a process.
[0013] it is illustrated in drawing 1 — as — the front face of the semiconductor substrate 1 — — for example, technique, such as plasma CVD, — for example, Si — O2 **** — the insulator layer 2 of the becoming substratum is formed this insulator layer 2 top — for example, Mo The lower thin film layer 3 which consists of Ti W, and Au **** — the becoming central layer 4 and Mo The up thin film layer 5 which consists of Ti W is formed by technique, such as a spatter, (the 1st process).
[0014] In this case, it is SiO2 by technique, such as plasma CVD, further. The pattern of a photoresist 7 is formed on the insulating thin film 6 of the top which forms the insulating thin film 6 which consists of Si N, Si ON, etc. (the 2nd process), and was formed in this way (the 3rd process).
[0015] The lower thin film layer 3, the central layer 4, the up thin film layer 5, and the insulating thin film 6 are layers which are wiring, each of the lower thin film layer 3, the central layer 4, and the up thin film layer 5 is formed in thickness of 10–200nm, 300–2000nm, and 10–200nm, respectively, and the topmost insulating thin film 6 is formed in thickness of 10–100nm.
[0016] A photoresist 7 is processed into a mask for this wiring layer for example, by the ion milling method at the configuration of wiring 3a, wiring 4a, wiring 5a, and wiring 6a, and wiring M of multilayer structure is formed (the 4th process).
[0017] Then, immersing [liquid / sublation / ashing for example by the oxygen plasma and] and washing processing according to a methanol, a pure water, etc. further remove the photoresist 7 which remains on wiring M.
[0018] Furthermore, as shown, for example in drawing 2 , an insulating layer 8 is formed on wiring M formed as mentioned above.
[0019] since the top of wiring M is covered by the insulating thin film 6 (wiring 6a) here in the case of this example — Mo of the bottom **** — there is no concern of oxidization by the oxygen plasma [in the elimination process of a series of above photoresists 7 in the becoming up thin film layer 5] or contamination
[0020] In the case of this example, ashing by sufficient time and the acid oxygen plasma treatment can be performed, and that is, taking a photoresist 7 by wiring M, to it, in case a photoresist 7 is removed, since the up thin film layer 5 (wiring 5a) is protected by the insulating thin film 6 (wiring 6a) can be finished completely. Furthermore, in case a photoresist 7 is removed, the up thin film layer 5 (wiring 5a) oxidizes, and does not pollute. Moreover, as the up thin film layer 5 (wiring 5a) is a process, it does not disappear.
[0021] Furthermore, the flattening of each class in the multilayer–interconnection structure which a cure, such as making the thickness of the up thin film layer 5 (wiring 5a) thick beyond the need in preparation for oxidization or disappearance, is unnecessary, and can suppress

the height dimension of wiring M, for example, carries out the laminating of two or more wiring M to two or more layers through an insulating layer 8 becomes easy.
[0022] consequently, Au from which the insulating layer 8 formed on wiring M constitutes wiring M **** — it originates in contacting directly the becoming central layer 4 (wiring 4a) etc., the failure of exfoliating from the concerned wiring M and the failure who originates in a left thing of a photoresist 7 etc. further are lost, and the yield of a semiconductor device improves certainly
[0023] Although invention made by this invention person above was concretely explained based on the example, it cannot be overemphasized by this invention that it can change variously in the domain which is not limited to the aforementioned example and does not deviate from the summary.
[0024]
[Effect of the Invention] It is as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0025] That is, according to the semiconductor device of this invention, the effect that sublation with a wiring of multilayer structure and a upside insulator layer can be prevented certainly is acquired. Moreover, the effect that the yield can be raised is acquired.
[0026] Moreover, according to the manufacture technique of the semiconductor device of this invention, the effect that sublation with a wiring of multilayer structure and a upside insulator layer can be prevented certainly is acquired. Moreover, the effect that sufficient photoresist elimination processing can be performed is acquired, without being anxious about trauma of a wiring etc. Moreover, the effect that the yield of a semiconductor device can be raised is acquired.

[Translation done.]